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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,428	08/20/2003	Brian Greg Montano	016295.1485	7000
23640	7590	09/19/2005		
BAKER BOTTS, LLP 910 LOUISIANA HOUSTON, TX 77002-4995			EXAMINER RODRIGUEZ, PAUL L	
			ART UNIT 2125	PAPER NUMBER

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,428	MONTANO ET AL.	
	Examiner	Art Unit Paul L. Rodriguez	2125

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 14 July 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

1. The amendment filed 7/14/05 has been received and considered. Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by O'Connor (U.S. Pat 5,894,571).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

The claimed invention reads on O'Connor as follows:

O'Connor discloses (claim 1, 10, 12, 14) a method for installing hardware components in installation locations a computer system (col. 2 lines 24-26, 44-46, 55-59, col. 3 lines 3-6, reference number 114, regarding claim 10 it is considered inherent that the computer system assembled would include a processor, memory and storage device), comprising compiling or

receiving a list of the hardware components (col. 2 lines 41-44, 53-54, col. 2 line 63 – col. 3 line 3, col. 4 lines 16-18), assigning an installation location for each hardware component of the computer system (col. 2 lines 25-26, Examiner considers a selected configuration would inherently include the install locations, col. 3 lines 1-2, col. 5 lines 4-5), evaluating each hardware component of the computer system to determine if the hardware component is compatible with respect to the other hardware components of the computer system, evaluating the compatibility of each hardware component of the computer system with respect to a base architecture of the computer system (col. 4 lines 38-55, col. 8 lines 20-26), displaying in graphical form the assigned installation locations of the hardware components of the computer system following a successful evaluation of the compatibility of the hardware components with respect to (a) the other hardware components of the computer system and (b) the base architecture of the computer system (col. 2 lines 41-44, 53-54, col. 2 line 63 – col. 3 line 3, col. 4 lines 46-50, col. 4 line 56 – col. 5 line 7, a list is considered a graphical form), and installing the hardware components according to the assigned installation locations (col. 5 lines 5-7), (claim 2) wherein the step of evaluating the compatibility of each hardware component of the computer system with respect to the base architecture of the computer system further comprises the step of evaluating the compatibility of the installation location with respect to a selected hardware component (col. 4 lines 46-50), (claim 3, 11, 13) wherein the list of hardware components includes custom hardware components selected for installation by a customer of the computer system (col. 2 lines 39-44, 50-55, col. 4 lines 14-18, 38-45), (claim 4) wherein the step of compiling a list of hardware components comprises the step of generating an architecture resource file that includes an identification of the hardware components and base architecture of the computer system (col. 3 lines 12-21, col. 5 lines 66-67), (claim 5) further comprising the step

of displaying instructions identifying incompatible hardware components (col. 4 lines 38-55, col. 5 lines 7-10, col. 8 lines 20-26), (claim 6) wherein the step of compiling a list of hardware components comprises the step of receiving a customer order and generating a list of hardware components from the customer order (col. 2 lines 39-44, 50-55, col. 4 lines 38-60), (claims 7-9) further comprising the step of assigning an identification number to the computer system, wherein the identification number is a serial number, wherein the identification number identifies assembled hardware components (col. 3 lines 12-21), (claims 15, 17 19) wherein the hardware components comprise hardware cards (considered inherent to a computer system) and (claim 16, 18 and 20) wherein the hardware components comprise memory modules (again considered inherent to a computer system). Examiner would like to point out that any reference to specific figures, columns and lines should not be considered limiting in any way, the entire reference is considered to provide disclosure relating to the claimed invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-14, 16, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (U.S. Pat 6,446,243).

Huang et al teaches (claim 1) a method for installing hardware components in installation locations in a computer system (reference number 20, col. 4 lines 11-55, a circuit or system considered a computer system), comprising compiling a list of the hardware components (reference number 10-14, col. 4 lines 11-33, col. 5 lines 5-26), assigning an installation location for each hardware component of the computer system (col. 4 lines 42-46, col. 5 lines 15-26), evaluating each hardware component of the computer system to determine if the hardware component is compatible with respect to other hardware components of the computer system (abstract, figure 5, col. 4 lines 30-64), evaluating the compatibility of each hardware component of the computer system with respect to a base architecture of the computer system (abstract, figure 5, col. 4 lines 30-64), displaying in graphical form the assigned installation locations of hardware components of the computer system following a successful evaluation of the compatibility of the hardware components with respect to (a) the other hardware components of the computer system and (b) the base architecture of the computer system (col. 4 lines 50-55, col. 5 lines 27-35) and installing the hardware components according to the assigned installation locations (reference number 20), (claim 10) a computer system, comprising a processor; a memory; a storage device; the computer system having been manufactured in accordance with a manufacturing process (abstract, col. 4 lines 11-55), (claim 12) a method for assigning installation locations for hardware components in a computer system (reference number 10-16,

col. 4 lines 42-46, col. 5 lines 15-26) comprising the steps of receiving a list of hardware components (reference number 10), evaluating the compatibility of each hardware component (abstract, figure 5, col. 4 lines 30-64), selecting an installation location for each hardware component in the computer system (reference numbers 16-18), and displaying a graphical representation of the installation locations of the hardware components of the computer system (col. 4 lines 50-55, col. 5 lines 27-35). Regarding dependent claims (claim 2, 14) wherein the step of evaluating the compatibility of each hardware component of the computer system with respect to the base architecture of the computer system further comprises the step of evaluating the compatibility of the installation location with respect to a selected hardware component (reference number 18), (claim 3) wherein the list of hardware components includes custom hardware components selected for installation by a customer of the computer system (obvious is a system were being designed it would be for an intended purpose of for a customer), (claim 4) wherein the step of compiling a list of hardware components comprises the step of generating an architecture resource file that includes an identification of the hardware components and base architecture of the computer system (reference number 510 HDL file), (claim 5) further comprising the step of displaying instructions identifying incompatible hardware components (col. 6 lines 37-43), (claim 6, 11, 13) wherein the step of compiling a list of hardware components comprises the step of receiving a customer order and generating a list of hardware components from the customer order (obvious), (claim 7-9) further comprising the step of assigning an identification number to the components (col. 5 lines 8-38), (claim 16, 18, 20), wherein components comprise memory modules (reference numbers 520, 530). Examiner would like to point out that any reference to specific figures, columns and lines should not be

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considered limiting in any way, the entire reference is considered to provide disclosure relating to the claimed invention.

Huang et al fails to use specific language and terms recited by the instant claims, the Examiner considers the Huang et al to encompass a teaching broad enough to read on the claimed invention.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the method and system for design, verification and assembly of a circuit or a system of Huang et al for a method and system for installing hardware components in a computer system, evaluating compatibility and installing or producing the components as claimed above because Huang et al teaches a computer assisted method and apparatus for design verification and assembly of circuits and systems with advantages relating to circuit design and verification by identifying potential mistakes during integration and testing (col. 3 lines 16-44). While the circuit or system is not identified as a personal computer, an integrated circuit can be considered a computer system.

Response to Arguments

6. Applicant's arguments filed 7/14/05 have been fully considered but they are not persuasive.

Regarding the claim rejections and rejections under 35 USC 112 2nd. The amendment to the claims corrected the cited deficiencies and the rejections and objections are withdrawn. However the art rejections are maintained.

Applicant argues that O'connor does not disclose the step of displaying installation locations in graphical form. It is the Examiners position that because the hardware list is entered into a computer, the computer has a user interface and it is well known that user interfaces use

graphical user interfaces to allow an operator to use a system. The Examiner considers the hardware list in the computer environment to read on displaying in graphical form the installation locations, even if only in a text format, it is still in a graphical form and because the system uses the hardware list to plan the component assembly, the Examiner considers any display of the assembly to also be a graphical display.

Regarding applicant's reference to another office action presented in a related case. While applicant's Exhibit A represents the position of one Examiner, this Examiner does not share that same position.

Regarding claims 10 and 12 and in reference to Examiner Day. This Examiner, the one or record for the instant application does not share the opinion of Examiner Day and the rejection is maintained. Examiner would also like to point out that claim 10 is a product by process claim. According to the MPEP, "A claim to a device, apparatus, manufacture, or composition of matter may contain a reference to the process in which it is intended to be used without being objectionable under 35 USC 112, second paragraph, so long as it is clear that the claim is directed to the product and not the process" and also states that if the claim is claiming both the product and the process, the claim should be rejected under by 35 USC 112 and also 35 USC 101.

Regarding Huang, applicant argues, "Huang is not directed to the same technology." As applicant points out, Huang is directed to VLSI verification and circuit design. Examiner considers a VLSI "Very Large Scale Integration – circuit" to read on a computer system. VLSI chips are known to be fully functioning computing circuits, all on one device and are considered by the Examiner to read on a computer system, see reference number 520 which teaches the

elements of control, memory, register and data path, which are all components of a computer system.

Applicant argues that their invention is directed to determining and displaying compatible installation locations for hardware in the computer system. The computer implemented apparatus of Huang generates a physical layout after the design is checked, col. 4 lines 50-55 and figure 7 is described as “Graphical network nodes”, representing functional circuit entities, Huang also teaches in the background and in relation to figure 1, that prior to manufacturing “physical layouts” is determined. Also, steps 520-660 deal with order and placement of components on the system VLSI. While there is no specific recitation of the claim language, Huang teaches graphical display of the layout and install locations of control sections are determined.

Applicant states that the Examiner relied upon col. 4 lines 42-46 to support the rejection of the limitation directed to “displaying in graphical form...” Examiner actually referred to col. 4 lines 50-55, col. 5 lines 27-35. Col. 4 lines 50-55 teaches simulator outputs are checked for proper function development, proceeds to generate physical layouts for fabrication. Examiner relies upon this passage to teach the assigned installation locations of the system are determined. Output from the simulator must also be in a form usable by a person, therefore a displayed output of some kind is inherent. Finally, col. 5 lines 27-55 teach “Graphical network nodes” which support “displaying in graphical form”. Based upon these teachings, the Examiner concludes that the limitations of “displaying in graphical form...installation locations...of the computer system” are taught. Col. 4 lines 42-46 were used to support the rejection of a different limitation.

Applicant argues that there is no mention in Huang where sub-blocks are to be installed in the computer system. While Huang doesn’t specifically recite that the sub-blocks are

installed, they are manufactured/fabricated in step 20 and because they are fabricated in the VLSI, they are in effect “installed components in the computer system”.

Applicant argues that the blocks in Huang are not hardware. It is the Examiners position that a fabricated VLSI consists of hardware elements once fabricated, a flip-flop and register are not “computational functions”, they are hardware components, components that are present in the manufactured VLSI device.

Applicant argues that Figure 3 of Huang only shows a representation for the interactions of function and not installation locations of components. While Examiner agrees that figure 3 is a graphical form of components, Examiner also relies upon reference number 18, which teaches a physical layout of the design prior to fabrication. Again, the combined teachings side with the Examiner on the obvious type rejection.

Applicant argues that Huang does not evaluate compatibility of hardware components. Examiner disagrees, this is one of the major functions of Huang, the design is simulated for design verification, steps 520-550, evaluate the compatibility, and step 14 in figure 1 also evaluates design, arguments not persuasive.

Applicant argues that Huang does not disclose the step of determining if any one hardware component is compatible with any other. Examiner disagrees, all components are evaluated therefore, any one component with any other component is supported.

The Examiner considers the combined teachings found within one single reference of Huang adequate to support an obviousness rejection. Examiner agrees that the specific language found in the claims is not recited in the Huang reference, however one of ordinary skill in the art would consider the display step to be obvious. All claims stand rejected.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Curran et al (U.S. Pat 6,898,580) teaches a computer design system with selection evaluation.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul L. Rodriguez whose telephone number is (571) 272-3753. The examiner can normally be reached on 6:00 - 4:30 T-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Paul L Rodriguez
Primary Examiner
Art Unit 2125